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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/554,106	08/28/2006	Hiroya Kobayashi	046124-5433	6587

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EXAMINER	
AGGARWAL, YOGESH K	

ART UNIT	PAPER NUMBER
2622	

NOTIFICATION DATE	DELIVERY MODE
01/12/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

DBRIPDocket@dbr.com
penelope.mongelluzzo@dbr.com

Office Action Summary	Application No.	Applicant(s)	
	10/554,106	KOBAYASHI ET AL.	
	Examiner	Art Unit	
	YOGESH K. AGGARWAL	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4 and 5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4 and 5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/02/2010 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 2, 4 and 5 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weale (US Patent # 6,049,470) in view of Ueda (US Patent # 6,122,009).

[Claim 1]

Weale teaches a solid-state imaging apparatus (figures 1 and 2) comprising:

a solid-state imaging element, having an energy ray sensitive portion (CCD imaging sensor has an energy ray sensitive portion as shown sense “N" in order to convert image signals into light, col. 2 lines 39-47 col. 3 lines 1-6, col. 3 lines 55-67) ;

a signal processing circuit (MOS transistor, bipolar transistor “Q” and load resistor “R”) , processing signals output from said solid-state imaging element (CCD outputs charge packets readout in sequence, see col. 4 lines 10-18) and including a load resistor (chip resistor R) electrically connected to an output terminal of the solid- state imaging element (See figure 2 wherein the CCD "S" is connected to the resistor "R" via gold bonding wire "G", col. 3 lines 28-33) and

a package (case “C” in figure 2), housing the solid-state imaging element and the signal processing circuit, wherein the load resistor (chip resistor R) and the output terminal of the solid-state imaging element are electrically and directly connected via a bonding wire (See figure 2 wherein the CCD "S" is directly connected to the resistor "R" via gold bonding wire "G", col. 3 lines 28-33)

Weale fails to teach wherein the signal processing circuit is positioned at a planar portion of the package that differs from a planar portion at which the solid-state imaging element is positioned and is positioned alongside the solid-state imaging element when viewed from a direction perpendicular to the planar portion at which the solid-state imaging element is positioned.

However Ueda teaches a solid-state imaging apparatus comprising (figure 34) a solid-state imaging element (image sensor 12) and a signal processing circuits (A/D converter 14), processing signals output from said solid-state imaging element, wherein the signal processing circuit is positioned at a planar portion of the package that differ from a planar portion at which the solid-state imaging element is positioned when viewed from a direction perpendicular to the planar portion at which the solid-state imaging element is positioned (figure 34).

Therefore taking the combined teachings of Weale and Ueda, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have the signal processing circuit is positioned at a planar portion of the package that differ from a planar portion at which the solid-state imaging element is positioned when viewed from a direction perpendicular to the planar portion at which the solid-state imaging element is positioned as taught in Ueda to be used in the system of Weale in order for the image processing circuit and the solid state sensor to be assembled into a smaller space on different planes side by side which leads to miniaturization of the overall circuit and therefore less costly.

[Claim 2]

Weale teaches a solid-state imaging apparatus (figures 1 and 2) comprising:

a solid-state imaging element, having an energy ray sensitive portion (CCD imaging sensor has an energy ray sensitive portion as shown sense “N" in order to convert image signals into light, col. 2 lines 39-47 col. 3 lines 1-6, col. 3 lines 55-67) ;

a signal processing circuit (MOS transistor, bipolar transistor “Q” and load resistor “R”) , processing signals output from said solid-state imaging element (CCD outputs charge packets readout in sequence, see col. 4 lines 10-18) and including a load resistor (chip resistor R) electrically connected to an output terminal of the solid- state imaging element (See figure 2 wherein the CCD "S" is connected to the resistor "R" via gold bonding wire "G", col. 3 lines 28-33) and

a package (case “C” in figure 2), housing the solid-state imaging element and the signal processing circuit (See figure 2 wherein the CCD "S" and the resistor "R" and the bipolar transistor are encased in case “C”) and wherein the load resistor and the output terminal of the

solid-state imaging element are electrically and directly connected via a bonding wire (See figure 2 wherein the CCD "S" is directly connected to the resistor "R" via gold bonding wire "G", col. 3 lines 28-33),

Weale fails to teach wherein the signal processing circuit is positioned at a planar portion of the package that differs from a planar portion at which the solid-state imaging element is positioned and is positioned alongside the solid-state imaging element when viewed from a direction perpendicular to the planar portion at which the solid-state imaging element is positioned.

However Ueda teaches a solid-state imaging apparatus comprising (figure 34) a solid-state imaging element (image sensor 12) and a signal processing circuits (A/D converter 14), processing signals output from said solid-state imaging element, wherein the signal processing circuit is positioned at a planar portion of the package that differ from a planar portion at which the solid-state imaging element is positioned when viewed from a direction perpendicular to the planar portion at which the solid-state imaging element is positioned (figure 34).

Therefore taking the combined teachings of Weale and Ueda, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have the signal processing circuit is positioned at a planar portion of the package that differ from a planar portion at which the solid-state imaging element is positioned when viewed from a direction perpendicular to the planar portion at which the solid-state imaging element is positioned as taught in Ueda to be used in the system of Weale in order for the image processing circuit and the solid state sensor to be assembled into a smaller space on different planes side by side which leads to miniaturization of the overall circuit and therefore less costly.

[Claim 5]

Weale in view of Ueda teach all the limitations of claims 1 or 2. However Weale further teaches wherein the signal processing circuit further includes a field-effect transistor (MOS) making up a source follower circuit with the load resistor (col. 3 lines 1-6, col. 3 lines 44-48).

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Weale (US Patent # 6,049,470), Ueda (US Patent # 6,122,009) and in further view of Throngnumchai et al. (US Patent # 5,705,807).

[Claim 4]

Weale in view of Ueda teach all the limitations of claims 1 or 2. However Weale further teaches wherein the signal processing circuit comprises a load resistor one end of which the load resistor is electrically connected to an output terminal of the solid-state imaging element and the other end of the load resistor is grounded (see figure 2 and col. 3 lines 15-27); and wherein the signal processing circuit further includes an amplifier, having a bipolar transistor (Q, col. 4 lines 19-20) that is electrically connected to the output terminal of the solid-state imaging element (see figure 2).

Weale in view of Ueda fail to teach wherein the signal processing circuit further includes a buffer amplifier.

However Throngnumchai teaches in figure 45 a photodiode 31 and a buffer amplifier (32), having a bipolar transistor (M1 or M2) that is electrically connected to the output terminal of the solid-state imaging element 31 (col. 29 lines 19-48, figure 45).

Therefore taking the combined teachings of Weale, Ueda and Throngnumchai, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have a

buffer amplifier so that the analog output signals are amplified in a comparatively noise-free environment inside the integrated package.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOGESH K. AGGARWAL whose telephone number is (571)272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571)-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Yogesh K Aggarwal/
Primary Examiner, Art Unit 2622